CLAIMS

What is claimed is:

1. A clock recovery circuit comprising:
   a. a transition detector that receives a plurality of data transitions of various data-transition types, the transition detector including a plurality of data-transition output terminals, each data-transition output terminal producing a data-transition signal in response to a respective one of the data-transition types;
   b. transition select logic having a plurality of select-logic input nodes, a select-logic output node, and select-logic control terminals, each select-logic input node coupled to a respective one of the data-transition output terminals, wherein the transition select logic conveys at least one of the data-transition signals from one a respective one of the select-logic input nodes to the select-logic output node in response to select-logic control signals to the select-logic control terminals; and
   c. a select-logic control circuit having control-circuit output terminals coupled to the select logic control terminals;
   wherein the select-logic control circuit issues transition select signals to the transition select logic via the select logic control terminals.

2. The clock recovery circuit of claim 1, wherein the select-logic control circuit issues the transition select signals in response to at least one of the data-transition signals.

3. The clock recovery circuit of claim 2, wherein the select-logic control circuit includes control-circuit input terminals coupled to respective ones of the data-transition output terminals.

4. The clock recovery circuit of claim 1, wherein the data-transition types include 2PAM and 4PAM data transitions.

5. The clock recovery circuit of claim 1, wherein the select-logic control circuit issues select-logic control signals that cause the transition select logic to select data transitions of a first type in the absence of a minimum number of data transitions of a second type.

6. The clock recovery circuit of claim 5, wherein the data transitions of the first type are 2PAM data transitions and the data transitions of the second type are 4PAM data transitions.

7. The clock recovery circuit of claim 1, further comprising a data sampler that samples a received data stream to provide a sampled data stream, the sampled data stream including the plurality of data transitions.

8. The clock recovery circuit of claim 7, further comprising a phase mixer coupled between the transition-select logic and the sampler, wherein the phase mixer provides a clock signal to the sampler.

9. The clock recovery circuit of claim 1, the select-logic control circuit including a transition analyzer that receives the data-transition signals.

10. The clock recovery circuit of claim 9, wherein the transition analyzer counts the data-transition signals associated with different ones of the data-transition types.

11. The clock recovery circuit of claim 9, wherein the transition analyzer examines patterns associated with at least one of the data-transition types.

12. The clock recovery circuit of claim 9, wherein the transition analyzer issues transition vectors based upon the data-transition signals.

13. The clock recover circuit of claim 12, the select-logic control circuit including a mode generator coupled between the transition analyzer and the transition select logic, wherein the mode generator issues transition select signals in response to the data-transition vectors.

14. A clock recovery method comprising:
    a. sampling a data stream using a receive clock to generate sampled data;
    b. monitoring the sampled data for data transitions of a plurality of possible data-transition types;
    c. automatically selecting a subset of the data transitions based upon the monitoring; and

d. adjusting the receive clock relative to the sampled data using the subset of the data transitions.

15. The clock recovery method of claim 14, wherein the data stream is a multi-level signal.

16. The clock recovery method of claim 15, wherein the data stream is a multi-PAM signal.

17. The clock recovery method of claim 14, wherein automatically selecting the subset of the data transitions includes determining whether the data stream is a multi-level signal.

18. The clock recovery method of claim 14, wherein automatically selecting the subset of the data transitions includes determining whether the data stream is a multi-PAM signal.

19. The clock recovery method of claim 14, wherein automatically selecting a subset of the data transitions comprises separating the data transitions into at least two of the data-transition types.

20. The clock recovery method of claim 19, wherein automatically selecting a subset of the data transitions comprises matching a sequence of at least one of the data-transition types to a pattern.

21. The clock recovery method of claim 19, wherein automatically selecting a subset of the data transitions

comprises counting data transitions of at least one of the data-transition types.

22. The clock recovery method of claim 19, wherein a majority of the data transitions are of a first of the data-transition types, the method further comprising adjusting the phase of the receive clock in response to the first data-transition type.

23. A clock recovery circuit comprising:

a. a transition detector that receives a plurality of data transitions of various data-transition types, the transition detector including a plurality of data-transition output terminals, each data-transition output terminal producing a data-transition signal in response to a respective one of the data-transition types;

b. transition select logic having a plurality of select-logic input nodes, a select-logic output node, and select-logic control terminals, each select-logic input node coupled to a respective one of the data-transition output terminals, wherein the transition select logic conveys at least one of the data-transition signals from one a respective one of the select-logic input nodes to the select-logic output node in response to select-logic control signals to the select-logic control terminals; and

c. control means connected to the select-logic control terminals, wherein the control means issues transition select signals to the transition select logic in response to the data transitions.

24. The clock recovery circuit of claim 23, wherein the transition select signals select a predominant one of the data-transition types.

25. A clock recovery circuit comprising:
    a. a transition detector that receives a plurality of data transitions of various data-transition types;
    b. transition select logic that receives the data transitions and that conveys a feedback signal in response to at least one of the data-transition types; and
    c. a select-logic control circuit that controls the transition select logic to select the at least one of the data-transition types based on the received data transitions.

26. The clock recovery circuit of claim 25, wherein the select-logic control circuit controls the transition select logic to select a predominate data-transition type.

27. The clock recovery circuit of claim 25, wherein the select-logic control circuit repeatedly controls the transition select logic to convey the feedback signal in response to different data-transition types.

28. A clock recovery circuit comprising:
    a. a transition detector that receives a plurality of data transitions of various data-transition types and produces unique data-transition signals in

response to a respective ones of the data-transition types; and

b. select logic that selects ones of the data-transition signals based upon the received data-transition types.

29. The clock recovery circuit of claim 28, wherein the select logic includes a select-logic control circuit and transition select logic.

30. The clock recovery circuit of claim 28, wherein the select-logic control circuit issues transition select signals to the transition select logic in response to at least one of the data-transition signals.

31. The clock recovery circuit of claim 30, wherein the transition detector includes a plurality of output nodes, wherein each output node conveys one type of the data-transition signals.

32. The clock recovery circuit of claim 30, wherein the select-logic control circuit includes control-circuit input terminals coupled to respective ones of the data-transition output terminals.

33. The clock recovery circuit of claim 28, wherein the data-transition types include 2PAM and 4PAM data transitions.

34. The clock recovery circuit of claim 28, wherein the select-logic control circuit issues select-logic control signals that cause the transition select logic to select

data transitions of a first type in the absence of a minimum number of data transitions of a second type.

35. The clock recovery circuit of claim 34, wherein the data transitions of the first type are 2PAM data transitions and the data transitions of the second type are 4PAM data transitions.

36. The clock recovery circuit of claim 28, further comprising a data sampler that samples a received data stream to provide a sampled data stream, the sampled data stream including the plurality of data transitions.

37. The clock recovery circuit of claim 36, further comprising a phase mixer coupled between the select logic and the sampler, wherein the phase detector provides a clock signal to the sampler.

38. The clock recovery circuit of claim 28, the select logic including a transition analyzer that receives the data-transition signals.

39. The clock recovery circuit of claim 38, wherein the transition analyzer counts the data-transition signals associated with different ones of the data-transition types.

40. The clock recovery circuit of claim 38, wherein the transition analyzer examines patterns associated with at least one of the data-transition types.

41. The clock recovery circuit of claim 38, wherein the transition analyzer issues transition vectors based upon the data-transition signals.

42. The clock recovery circuit of claim 40, wherein the select logic includes a mode generator coupled between the transition analyzer and the transition select logic, and wherein the mode generator issues transition select signals in response to the data-transition vectors.